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STUDY ON NONLINEAR HEAT TRANSFER EFFECT IN THE LOCK-IN THERMOGRAPHY FOR DEFECTS CHARACTERIZATION ON A THREE-DIMENSIONAL INTEGRATED CIRCUIT

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ABSTRACT

The use of the lock-in thermography (LIT) as a non-destructive evaluation technique is becoming increasingly attractive for detecting and characterizing the defects such as the shorts and resistive opens in a 3D package or stacked IC [1,2]. According to this trend, the study for improving the performance of the LIT system is required such as synchronous undersampling method [3]. One of the performance degradation factors of the LIT system is nonlinear distortion effects. Although the heat action is applied periodically, the resulting surface temperature is not synchronized with the periodic heating due to nonlinear heat transfer. A new approach to overcome unsynchronized result is proposed in one-dimensional systems [4]. In this study, we developed the 3D FE model of TSV structure with silicon chip integration and experimentally validated our FE model using measured current–voltage (I–V) and lock-in thermography (LIT) measurements in order to analysis nonlinear heat transfer. From the finite element analysis, the thermal distributions including nonlinear heat transfer in the TSV model and phase angle for the lock-in frequency are calculated and compared with experimental results of a TSV-based 3D IC sample.

KEYWORDS: Lock-in thermography, Non-destructive testing, 3D integrated circuit