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Fault Isolation of Heat Source Chip using Infrared Microscope

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Abstract

Measurement and depth estimation of thermally active buried heating source in stacked die architectures were performed by using the phase image obtained from infrared microscopic sensor. Highly sensitive infrared images were measured and post-processed using a lock-in method. By applying the lock-in method to infrared images, the detection sensitivity and signal to noise ratio were enhanced by the phase-sensitive narrow-band filtering effect. Operational principle of lock-in method concerning the thermal wave propagation through different material multi-layers was discussed and it was demonstrated that the phase information of thermal emission from silicon wafer sample can provides the good metrics about the depth of heat source. In addition, a photothermal model was implemented to evaluate the behavior of thermal waves from multi stacked silicon wafer sample by comparing a calculated depth with real one. Results showed that the infrared microscopic sensor technique with lock-in method and resultant phase information have a good potential in the application of the fault isolation and its depth estimation for the stacked die devices, especially in the packaged semiconductor.

1. Introduction

The complexity of microelectronic devices has been increased while the dimension and power consumption of their basic components such as transistors reversely have been reduced, and a semiconductor industry has focused on increasing transistor density by stacking transistors in 3D geometry. Moreover, the need of expanded functionality and faster connections has triggered the semiconductor industry to develop complex 3D package technology such as System-in-Package (SiP), wafer-level packaging and through-silicon-via (TSV) [1]. Although the 3 dimensional integrated circuit (3D-IC) allowing the reduction of form factor and lower power consumption with higher data transmission speed has been developed, the tasks about fault isolation (FI) and failure analysis (FA) are being more complex due to the difficulties of imaging through metal layers and semiconductor materials [2]. Many of the possible faults in microelectronic devices are connected with local heat dissipation, such as electrical shorts, oxide or junction breakdowns, high resistive opens, latch-ups, and many more [3].

Conventional standard method of non-destructive faults isolation such as photon emission microscopy or liquid crystal thermography showed the limitations because a direct optical access was not available to the 3D-IC structures. It is most important concerns that defects can be buried at deeper die or interconnect levels in the multi-stacked microelectronic devices. As a subsequent destructive inspection method, the removal of the individual staked dies using mechanical or chemical preparation tools are commonly performed, however this method is a time-consuming work and can induces an additional secondary defects, reducing FA success rate [4]. Thus, some researches into the non-destructive faults isolation of 3D-IC have been undertaken by the semiconductor industry. Magnetic Field Imaging (MFI) technique which uses a superconducting quantum interference device (SQUID) as the sensing element is considered as one of candidates for the faults isolation techniques of complex 3D interconnected devices because the low-frequency magnetic field generated by the currents in the DUT is not affected through the various materials used in device fabrication [5]. In addition, it is well-known that this technique is not affected by the number of layers. However, measurements based on a raster scanning consume a relatively long work time, and multiple predetermined steps such as standard inversion technique is certainly needed to acquire an image of the magnetic field distribution [6, 7].

Conventional time domain reflectometry (TDR) is also commonly known as a well established technique which can typically localize an open or short fault to within 500 μm of the defect for the fault isolation within the semiconductor industry. However, this level of fault localization is not sufficient in advanced 3D IC packages due to the increased complexity and the reduction in physical package size, hence, the ability to isolate the exact fault location is essentially needed to shorten the failure analysis cycle time. Therefore, an electro optical terahertz pulse reflectometry (EOTPR) which isolate faults in advanced 3D IC packages to an accuracy of 20 μm has been developed, and it was observed that the fault isolation accuracy of EOTPR was improved by its high measurement bandwidth, extremely low time base jitter and high time base resolution [8]. Nonetheless, these electrical characteristics analysis methods including both TDR and EOTPR certainly require the equivalent circuit model of test sample to obtain an accurate location or distance of fault location. Also, the technique needs to involve the further destructive investigation of the sample to confirm the results from the TDR or EOTPR.

In addition to the above technologies, various applications of infrared microscopic sensor have been explored to analyze the thermal characterization of electronic devices. This technique is useful not only for measuring the temperature on the surfaces of objects but also for detecting subsurface or internal heat intrusions within objects, which

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might serve as sensitive indicators of faults in 3D-IC. This non-contact technique which utilizes naturally emitted infrared radiation from a sample can provide a real time thermal image of device surface. However, the devices should be coated with a high emissivity coating material to obtain more accurate surface temperatures as well as the spatial resolution is limited to around 3 μm. In addition, the infrared microscopic sensor technique also has some limitations caused by the measurement sensitivity [9]. However, the limitations of faults isolation using infrared microscopic sensor technique have significantly been overcome by employing a lock-in method. It was demonstrated from several studies that the detection sensitivity was greatly enhanced by applying lock-in method into infrared thermal sensing technique [10, 11, 12, 13]. The idea of this phase sensitive modulated thermography technique was first presented by using the AGEMA Thermovision 900 mirror scanner thermocamera which was the infrared camera with lock-in function. The noise equivalent temperature difference of the system was evaluated as 15 mK, and it was not significant improvements over previous techniques. After that, dynamic precision contact thermography was developed as the first lock-in thermography technique which able to detect temperature below 100 μK with a spatial resolution of approximately 30 μm. However, this contact method showed limitations in the non-destructive evaluation of materials or integrated circuits.

Since the late 1990 years, a highly sensitive infrared lock-in thermography system has been developed, and used in the several industries such as electronics, aircraft, and defense for the non-destructive thermo-mechanical investigations. This technique uses periodic excitation methods using thermal, vibration, or ultrasound waves; the resulting amplitude and phase information represents an indication of damage including both the size and the depth of the damage. Wu and Busse [13] described the principle of lock-in thermography and demonstrated that lock-in thermography can eliminate disturbances such as surrounding reflections, local variations of the surface optical absorption and the infrared emission coefficient, and inhomogeneous illumination by heating sources. Choi et al [14] evaluated the sizes and locations of subsurface defects using lock-in infrared thermography and showed that a phase difference between the defect area and the healthy area indicates the qualitative location and size of the defect.

In this study, we constructed an infrared lock-in microscope system consisting of a mid-IR range (1.5-5 μm) infrared camera and current-voltage source meter. We then analyzed the infrared thermal signals from chip sample to identify a heat source and depth of it using a lock-in thermography technique. In this method, a periodic bias was generated and supplied to chip sample using current-voltage source meter, and the characteristic thermal response of objects was analyzed on the basis of phase images. In addition, a photothermal model of periodic thermal waves was employed to estimate the depth of heat source in chip sample and compare the phase information of measurements with that of photothermal model.

2. Material and methods

2.1. Wafer stacked heat source chip

Figure 1 shows a wafer stacked chip sample which contains a meander of copper material inside of it. The copper meander was locally opened in order to employ a heat source made of poly resister as shown in figure 2. Figure 3 shows the cross section of three different chip samples which are stacked by one, two and three silicon wafers. The thicknesses of one silicon wafer and adhesive were measured using SEM and average of them was observed as 667 μm and 4 μm, respectively. In addition, heat conductivity, specific heat capacity and density of stacked wafer and adhesive are known as 149 W/m·K, 0.71 J/g·K, 2.33 g/cm^3 and 0.14 W/m·K, 1.11 J/g·K, 1.25 g/cm^3 respectively.

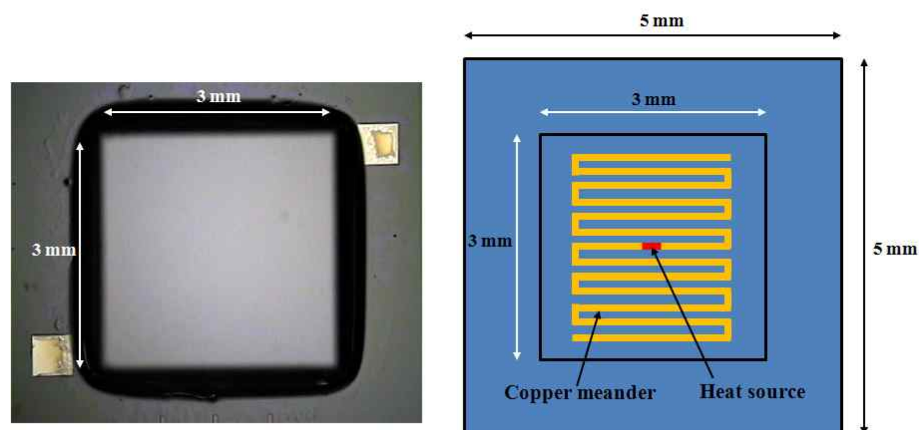

Fig. 1. *Wafer stacked heat source chip specimen*

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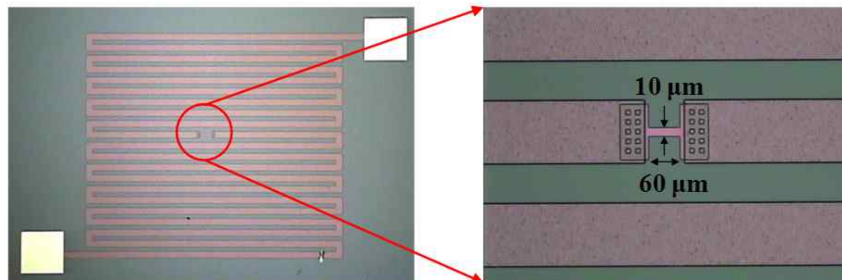

Fig. 2. *The generation of heat source by using local modification. A copper line is opened locally and poly resister is connected to create a local high ohmic heating*

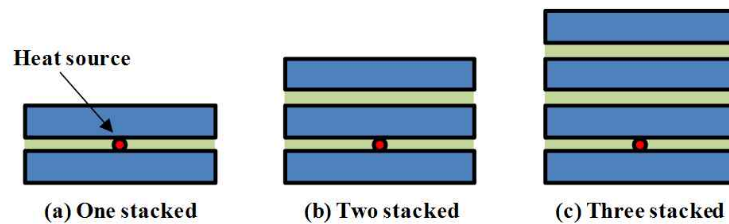

Fig. 3. *Cross section of three different chip samples*

2.2. Infrared lock-in microscope system

Figure 4 shows an infrared lock-in microscope system used for the measurement of thermal emissions from chip samples. It is consisted of a mid-infrared camera, infrared objective lens, and current-voltage source meter. Thermal images were taken using an infrared camera (SC7600, FLIR Systems, USA) that has a 640 × 512 pixel resolution and a sensitivity of 1.5–5 μm spectral range. The detector in the scanner unit was indium antimonide (InSb) and cooled by an integrated stirling cooler. Temperature sensitivity was 18 mK at 25°C. An infrared objective lens with a 3.2 × 2.5 mm field of view (IFOV: 5 μm, spectral band: 3.5-5 μm) was used. A current-voltage source meter (2602B, Keithley Instruments Inc., USA) was operated by a computer system to control a lock-in frequency, voltage amplitude and duty rate of bias signal.

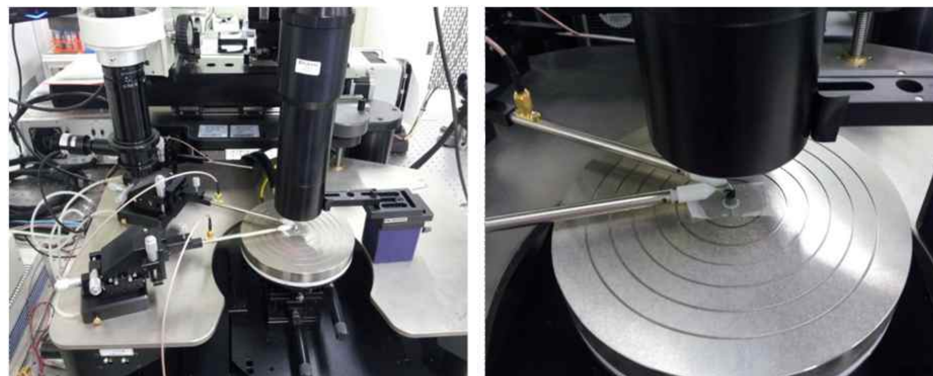

Fig. 4. *Infrared lock-in microscope system*

2.3. Infrared lock-in method

Periodical bias supplied to wafer stacked chip sample induce the modulated thermal emissions from the heat source of it. The modulated thermal emissions at the surface can be modified by the thermal and physical properties of materials which configure a test sample. Especially, the pixel-based phases of modulated thermal emissions are changed by the depth of heat source. An infrared sensor measures the modulated thermal emissions and then reconstructs a periodic wave pattern by picking up a series of thermal images with a step of T/n (where T is a lock-in period, and n is the number of samples per lock-in period). For the mathematical calculation of lock-in thermal signal, we applied the digital lock-in correlation method, which consists in averaging the product of the measured values and a set of weighting factors up to the total number of measured values. If the measurement is averaged over N lock-in periods, the digital lock-in correlation is expressed by the summation S expressed in Eq. (1) [15]. Figure 5 shows the working principle of lock-in thermography technique.

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$$S = \frac{1}{nN}\sum_{i=1}^{N}\ \sum_{j=1}^{n} K_j F_{i,j} \tag{1}$$

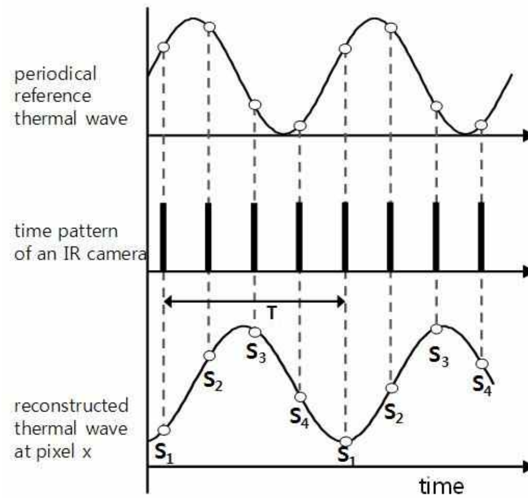

Fig. 5. *Working principle of Infrared lock-in thermography*

This digital lock-in correlation method uses two-channel correlation which means that there are two sets of correlation functions K_j, one approximating the sine component and the other approximating the cosine component. The first channel measures the components of the signal in-phase with the sine function, and the other channel measures the component in-phase with the cosine function, which is 90° phase-shifted to the sine function. If we assume that the amplitude of the detected signal is *A* and its phase is ϕ, we can define the measurement *F(t)* as $A\sin(2\pi f_{lock\text{-}in}t)\cos\phi + A\cos(2\pi f_{lock\text{-}in}t)\sin\phi$. After the signal *F(t)* has been processed with correlation functions $K^{0^\circ}(t)=2\sin(2\pi f_{lock\text{-}in}t)$ and $K^{90^\circ}(t)= 2\sin(2\pi f_{lock\text{-}in}t)$, the result of the two correlations over a complete number of periods will be $S^{0^\circ}=A\cos(\phi)$, $S^{90^\circ}=A\sin(\phi)$. S^{0° and S^{90° are usually called the in-phase signal and the quadrature signal, respectively. The phase-independent amplitude *A* and the signal phase ϕ will be retrieved from the two results S^{0° and S^{90° as shown in Eqs. (2) and (3) [15].

$$A = \sqrt{\left(S^{0^o}\right)^2 + \left(S^{90^o}\right)^2} \tag{2}$$

$$\phi = \arctan\left(\frac{S^{90^o}}{S^{0^o}}\right) \tag{3}$$

In a silicon stacked chip sample, silicon and adhesive can be thermal insulators inducing the phase shift of the thermal wave. Simply, the longer the depth between hot spot and sample surface, the higher the induced phase shift. It means that we can estimate the depth of hot spot with the measured phase information if the physical and thermal properties of sample are known. The parameter which describes the influence of the thermal properties of any material is called as thermal diffusion length (μ) which describes the damping of the thermal wave inside the material, and it is calculated by the thermal parameters heat conductivity (λ, W/m*K), specific heat capacity (C_p, J/g*K), density (ρ, g/cm³) and the applied lock- in frequency ($f_{lock\text{-}in}$, Hz) as shown in Eq. (4). In general, a thermal diffusion length is affected by not only the amplitude but also the phase of thermal wave because the thermal diffusion length can be considered as one of the damping factors of thermal waves. Also, time delay between the bias at the hot spot and the thermal response at the sample surface in increased with increasing lock-in frequency. Therefore, an increase of the phase as a function of the increased lock- in frequency can be expected. The relationship between phase and depth is shown in Eq. (5).

$$\mu = \sqrt{\frac{2 \times \lambda}{C_p \times \rho \times 2\pi f_{lock-in}}} \tag{4}$$

$$\phi = \frac{z}{\mu} \times 180/\pi \tag{5}$$

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3. Results and discussions

Registered thermal sequences were analyzed by lock-in thermography technique with different lock-in frequencies (1 Hz, 2 Hz, 3 Hz, 4 Hz, and 5 Hz). Figure 6 shows the phase images of two silicon wafer stacked chip sample which has a 1340 μm depth of hot spot. As shown in the figure 6, the fault location of hot spot which is not possible to observe with conventional infrared thermography was clearly detected. Figure 7 shows the phase at hot spot area for different applied lock-in frequencies and bias voltages (3, 4, 5 voltages). The phase difference increased with increasing lock-in frequencies as expected above. We also estimated the depth of hot spot in a silicon wafer stacked sample with the measured phases in figure 7 using the relationship between phase and depth which is described by Eq. (7). Lock-in frequencies were 1, 2, 3, 4 and 5 Hz and sample was biased with 4 voltages. Fig. 8 shows the estimated depth of hot spot, and the real depth of it was 1340 μm. As shown in figure 8, it was experimentally demonstrated that measured phase at hot spot was strongly correlated with its depth as described above.

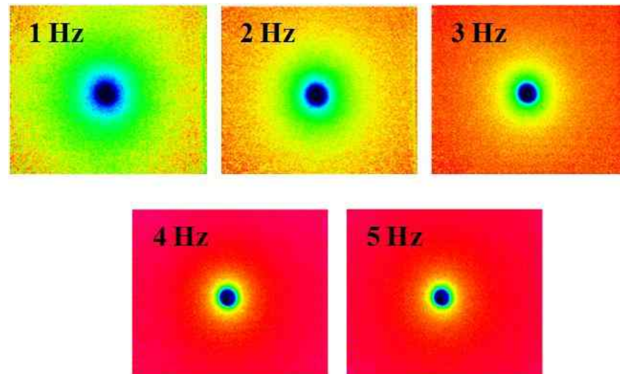

Fig. 6. *Phase images for different lock-in frequencies*

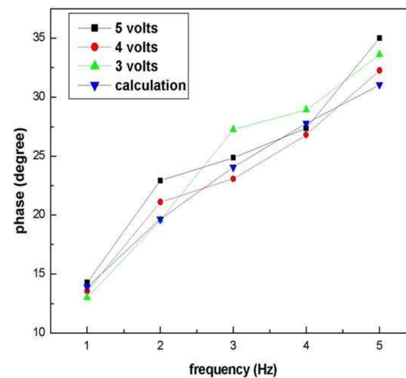

Fig. 7. *Phase of hot spot for different lock-in frequencies and bias voltage*

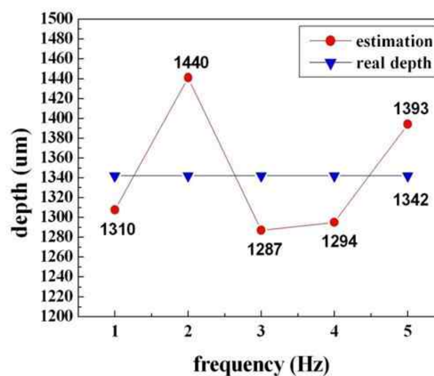

Fig. 8. *Estimated depths of heating source for lock-in frequencies*

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4. Conclusion

In this study, we registered thermal sequences of a silicon stacked wafer sample which includes an artificial hot spot fault, and analyzed its thermal wave using lock-in thermography technique with different lock-in frequencies. Results showed the feasibility of an infrared lock-in thermography for the detection of fault and estimation of depth of the hot spot in stacked die architecture. By adjusting the lock-in correlation method to measured thermal wave signals which recorded at different frequencies, effective NDE methodology of lock-in thermography for the isolation of the hot spot in stacked die architecture has been achieved through the phase information which is relatively insensitivity to non-uniform heating and local variation of the thermal emissivity. However, it is commonly known that the lock-in correlation method has a drawback in the selection of optimal lock-in frequency. This means that multiple tests are required to evaluate the whole range of depths at which a hot spot might exist. Moreover, the results reported in this work are obtained from artificially designed hot spot sample. In order to apply this method into a commercial package device especially in a TSV(Through Silicon Via) based package devices, the various influence of fault modes, a limitation of spatial, thermal resolution and any fault dependence of 3 dimensional geometry in package device should be investigated in near future.

Nevertheless, our experimental results have shown that the detection accuracy of hot spot using lock-in thermography was satisfactory. We expect that this application of relationship between phase and depth of hot spot in electronic device using infrared lock-in thermography has good potential as one of NDE methodology in 3D defect localization at fully package devices.

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