http://dx.doi.org/10.21611/qirt.2012.243

QIRT 2012

11th International Conference on
Quantitative InfraRed Thermography

Thermographic Measurements of Integrated Spiral Inductors

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Abstract

The aim of this paper is the measurement of small scale spatial temperature differences over the surface of integrated spiral inductors. In this current work the surface temperature distribution of spiral planar inductors on silicon substrate was measured. The measurements were conducted with the use of thermal infrared camera. Special care was taken in order to increase the spatial resolution of the thermographs. In order to verify the experimental results, measurements were compared with numerical simulations results.

1. Introduction

Nowadays wireless analog circuits rely strongly on the use of inductors for applications over a wide frequency range. For high frequencies the number of the inductances turns out to be small, and, therefore the inductors can be directly integrated on the substrate used for the rest of the circuitry. In such a way, it is possible to avoid the use of soldered external inductive components, e.g. spiral inductors [1][2][3][4][5].

The focus of this work is centered on spiral inductors integrated on silicon substrate. Owing to the small dimensions of the conducting traces comprising the coil, the series resistance will be relatively high. In such a case, a high imposed current can cause rather high joule losses and high power dissipation and therefore high temperature rise.

Integrated spiral coils are placed on top of a non-conducting passivation layer made of SiO_2, separating the inductors a bit from the conducting silicon substrate. Since SiO_2 has a much lower thermal conductivity than the silicon wafer, the inductor will have a higher thermal resistance. In addition, the silicon substrate is electrically conducting, and therefore alternating magnetic fields will give rise to eddy currents in the conducting silicon substrate.

In this current work, the surface temperature distribution of spiral planar inductors on silicon substrate was measured. Small scale spatial temperature differences were possible to be observed with the use of infrared thermographic equipment. A new technique was applied in an attempt to increase the spatial resolution of the thermographs. Extension tubes were applied to the thermographic equipment in order to increase the magnification [6]. Special treatment of the surface of the device under test was undertaken in order limit the effects of emissivity variations on the SiO_2 surface. Also, numerical analysis investigation of the temperature distribution of an integrated spiral inductor is presented. It must be emphasized that in electronics and to a major extend in microelectronics, small sized heat sources dissipating a small amount of power can give rise to relatively high temperatures [7][8][9]. Experimental results obtained with infrared microthermography will be presented in section 2. The inductor structure will be analyzed numerically in section 3. Final conclusions are closing the presentation.

2. Experimental measurements

Inductors have been integrated on a silicon wafer. A top view is depicted in fig.1. Conducting paths have a width of 12μm and separated by gaps of 2μm. The total dimensions can be roughly estimated as $160\times160\mu m^2$. Notice that the inductor is placed on top of a SiO_2 layer with a thickness of 5μm. This layer offers the needed passivation and electrical insulation between the inductor and the electrically conducting substrate. On the other hand, the SiO_2 layer has a much lower thermal conductivity $k = 1.38 W/mK$ than the Si substrate with a thermal conductivity $k = 148 W/mK$. Consequently, the passivation layer acts not only as a necessary electric insulation layer but also as an unwanted thermal insulation. Thus, the maximum allowable current is limited, as higher current will lead to higher joule losses and apparently to higher temperature increase.

http://dx.doi.org/10.21611/qirt.2012.243

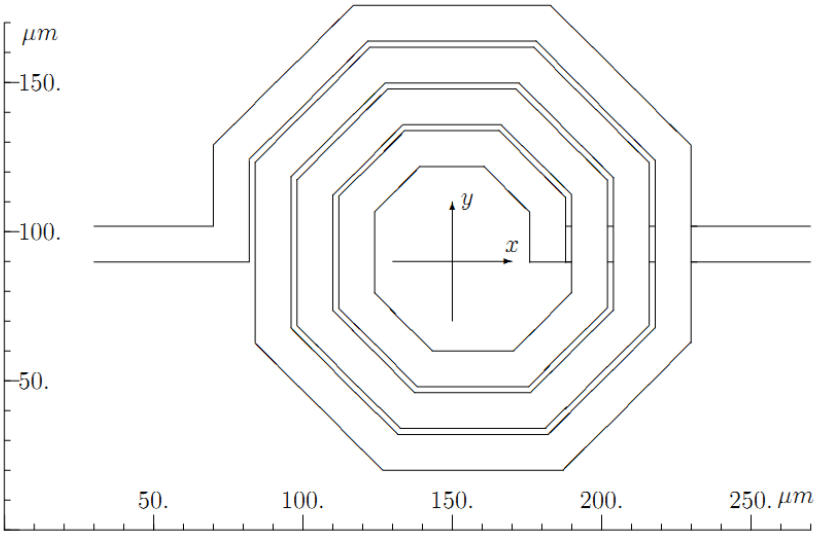

Fig. 1. *Schematic layout of an inductor*

During the experiments the temperatures were measured using an infrared thermographic camera (CEDIP). In order to guarantee a uniform surface emissivity, the surface had to be painted (fig.2). Hence in our experiments the temperature on the top of the paint coating will be measured. Therefore in both the simulations and the theoretical analysis section, this effect will also be taken into account. In order to make the small inductors visible for the infrared camera, specially designed extension rings were used. The spatial resolution turned out to be 7μm per pixel, while the width of the metal paths is 12 μm.

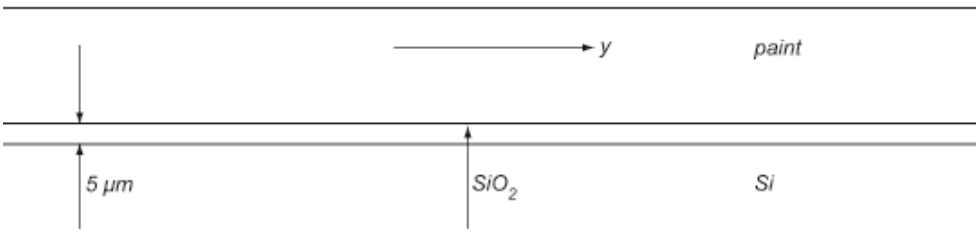

Fig. 2. *Cross sectional view of the integrated inductor*

During the measurements, a constant DC current of 64 mA was used to trigger an inductor. Taking into account a typical DC resistance value of 4 Ω, the total power dissipation was about 25 mW. In order to avoid the emissivity variations and externally generated temperature gradients, two measurements have been conducted. First of all, a sequence of two temperature distribution measurements was recorded; the temperature distribution with the power supply switched off followed by a second measurement with the power switched on. In each point the temperature difference ΔT was calculated. By doing so, we guaranteed that the resulting data are only due to the joule heating in the coil. Fig.3 displays ΔT along the *y*-axis (fig.1). It is easy to observe two peaks in the temperature distribution. The right peak ($y>0$) is a bit higher which is understandable because for $y>0$ one has 4 conductors whereas only 3 conductors are available for $y<0$. The distance between the two peaks is about 80 μm, which agrees quite well with the schematic layout of fig.1.

Taking into account the maximum temperature increase of 2K corresponding to a dissipation of $P = 25mW$, the thermal resistance of one coil can be calculated as:

$$R_{TH} = \frac{\Delta T_{\max}}{P} = 80\,K/W \tag{1}$$

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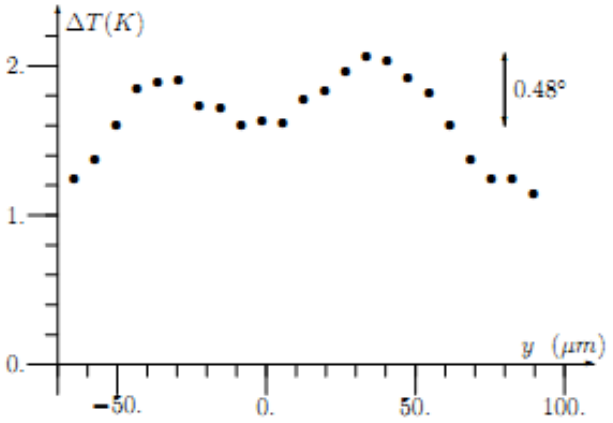

Fig. 3. *Experimental temperature measurements*

3. Numerical analysis

The structure of the integrated inductor has been simulated using the COMSOL software. The layout of the inductor as shown in fig.1 has been simulated electrically and thermally. First of all, an electric current of 64mA was fed through the inductor. The electric part of the simulation was used to get the current density distribution in the inductor coils from which the power density can be easily calculated. This power density is then used as the input of the subsequent thermal simulation.

It should be noticed that there is not only heat production in the windings of the inductor, but also in the two leads as they are made from the same materials and cross sectional dimensions. During the simulation the total power was still the same: 25 mW as used before.

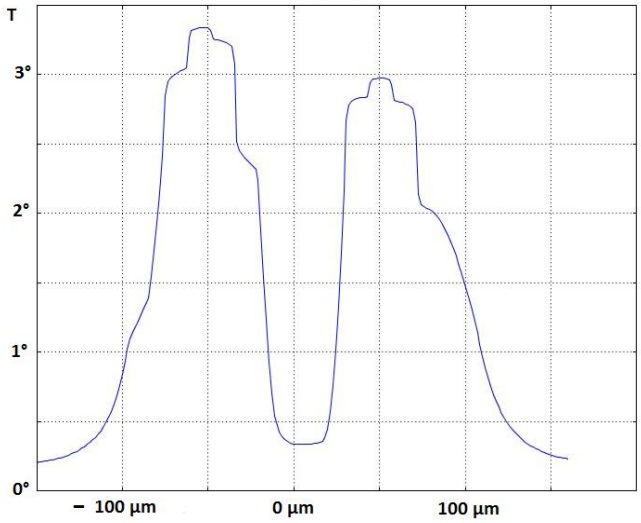

Fig. 4. *Numerically calculated temperature distribution over the inductor*

Fig.4 displays the temperature distribution of the coil itself calculated along the *x*-axis. If one proceeds from the left (-100 µm) one clearly observes 4 steps and further on to the right only 3. These steps clearly correspond to the individual windings. In between the windings, the temperature drops considerably. However, left and right from the windings the temperature drop is not that steep. This is due to the heat dissipation in the leads which are positioned on the *x*-axis. The temperature of the lead is also much less although they have exactly the same power dissipation per unit length. This is explained by the fact the windings are close to each other so that heat flow by conduction is inhibited. For the leads heat can flow by conduction on both sides.

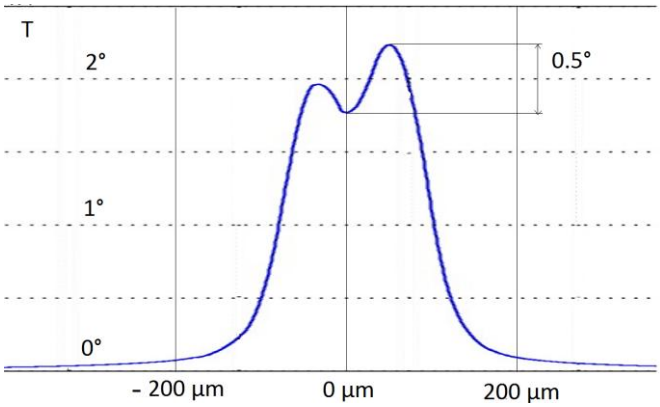

Fig. 5. *Numerically calculated temperature distribution on top of paint coating*

During the simulation a paint coating layers was taken into account as well. This layer with a thickness of 30 µm was assumed to have a thermal conductivity $k = 1\mathrm{W/m.K}$. The temperature on the top of the paint was calculated. A result is shown in fig.5. This time the temperature variation along the *y*-axis has been plotted, because the experimental measurements were also carried out in this direction. One should notice that the agreement with the experimental results is quite good. The peak on the right is somewhat higher because 4 windings are present there instead of 3. The dip in between the two peaks is quite small in agreement with the experiments.

The fluctuation of the temperature on top of the paint (fig.8) turns out to be around 0.5 degC. This value agrees well with the experimentally observed value of 0.48 degC (fig.3). Both curves (fig.3 and fig.8) show a maximum temperature increase around 2.0 degC.

It should be pointed out here that the temperatures obtained in this paper are quite small. This is due to the fact that a low power was used in order to prevent overheating during the experiments. In practical situations much higher power dissipations are possible.

4. Conclusion

It has been proved experimentally that it is possible to measure really small scale spatial temperature differences. In order to capture such small temperature variations additional optical rings extending the focus length were used. Further improvements are possible with the use of microscopic lenses.

Furthermore, it was shown that an integrated coil in an integrated circuit can have a thermal resistance up to 192 K/W. This value is rather high if one takes into account that integrated coils have rather large dimensions as compared to other components like transistors. A numerical analysis of the same problem proved that the fact the coil has to be deposited on a thin electric insulating layer of SiO_2 is the main reason for this high thermal resistance.

It was also proved that the deposition of paint on the integrated circuit in order to perform thermographic investigations has a major influence on the temperature measurements. Hence, the measurements have to be interpreted carefully in order to obtain the temperature of the integrated coil. The conclusion is that only a combination of measurements, analysis and simulations can provide this answer.

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