http://dx.doi.org/10.21611/qirt.2002.022

Thermal compact modeling for power electronic devices in D2Pak enclosures

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Abstract

In this paper, the compact modeling of power electronic devices is presented. Physical modeling using ANSYS is helpful to identify the compact model parameters. Thermographic measurements were applied to modeling validation. Compact models are very easy for computation, so they generate the results fast and with satisfactory accuracy.

1. Introduction

Thermal physical modeling using finite difference or finite element methods can be sometimes very complex and time consuming while computation. It is mainly because of thousands of nodes where the differential equations have to be fulfilled.

The different approach for thermal modeling assumes a very low number of boundary nodes, and one where the power is generated [3-5]. There is a heat transfer in between all nodes. It is necessary to know what is the portion of total power which is transferred to the ambient through each boundary node. Such modeling is known as compact modeling, and it is simple, and fast for computations. It can be quite helpful for engineering as well as for manufacturers of heat sources, because its precision is good enough and can be trimmed according the problem being solved.

In this paper we present compact modeling for power electronic devices encapsulated in D2Pak cases. It is well known fact that thermal and electrical quantities analogy (Table 1) allows to use electrical and electronic simulation packages in thermodynamics. Compact modeling is one the best example for using electronic solvers for thermal problems.

Table 1: *Thermal to electrical quantities conversion [1]*

Power P [W]	$\Rightarrow$	Current J [A]
Temperature T [K]	$\Rightarrow$	Voltage U [V]
Thermal resistance R_{TH} [K/W]	$\Rightarrow$	Electrical resistance. R [Ω]
Thermal capacitance C_{TH} [J/K]	$\Rightarrow$	Electrical capacitance. C [F]
Thermal conductivity λ [W/(m·K)]	$\Rightarrow$	Electrical conductivity σ [S/m]

2. Compact model for steady state

Compact models are derived from classical energy equation

$$\frac{\partial}{\partial x}\left(\lambda\frac{\partial T}{\partial x}\right)+\frac{\partial}{\partial y}\left(\lambda\frac{\partial T}{\partial y}\right)+\frac{\partial}{\partial z}\left(\lambda\frac{\partial T}{\partial z}\right)=-p_v \tag{1}$$

where: T – temperature, p_v – volumetric power density, λ – thermal conductivity.

Compact modeling as a simplified solution for heat transfer in solid bodies needs the following assumptions:

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a) the heat source is inside the solid body
b) the boundary of the body is segmented into the n parts with constant temperature T_i (i=1,..,n).

It is possible to prove [3,4], that if the eqn. (1) is linear, i.e.: λ does not depend on temperature, the temperature in heat source T_j is the linear combination of T_i ($i=1,..,n$), Additionally, temperature T_j is a function of power dissipated P, as expressed by:

$$T_j = R_{thJ0} \cdot P + \sum_{i=1}^{n} a_i T_i \tag{2}$$

where: R_{thJ0}, a_i – model parameters,

$P = \int_v P_v dv$ - power dissipated in the heat source with volume v

Assuming constant boundary temperature $T_o=T_i=const,$ and if the same heat flux is transferred through all part of the boundary, we can obtain additional equation, which has to be fulfilled:

$$\sum_{i=1}^{n} a_i = 1 \tag{3}$$

As a consequence, eqn. (2) is reduced to a form:

$$Tj = R_{thJ0} \cdot P + T_o \tag{4}$$

By assuming constant boundary temperature T_0, we can easily identify the first model's parameter R_{thJ0}. In practice, the heat transfer from the heat source to the ambient is much more complex, due to complex geometry of the investigated body and different boundary conditions. Temperature in this model is understood as the temperature difference between a given point and the ambient.

For the model completeness, one has to know how much power is dissipated to the ambient through the certain areas of the investigated heat source. We define the coefficients q_k describing the portions of power J_k transferred out of the surface in the *k-th* node. The temperature in the boundary nodes T_i , for $i=0,1,...,n$, are different, are therefore there is a heat flux in between. Such a flux in between *i-th* and *k-th* nodes is presented in the model by additional parameters $R_{i,k}$, which can be treated as the thermal resistance between given points.

Power transferred from *i-th* node to *k-th* one, if T_k=0 takes a form:

$$J_{i,k}=T_i/R_{i,k} \tag{5}$$

Obviously, the similar power is transferred in opposite direction, depending on T_k, and therefore $R_{i,k}= -R_{k,i}$. Finally, the energy conservation in *k-th* node allows to find the part of power J_k in this node dissipated to the ambient, as:

$$J_k = P \cdot q_k + \sum_{i=1}^{n} \frac{T_i}{R_{i,k}} \tag{6}$$

If the boundary temperature is constant, and $T_i=0$ in all nodes $(i=0,1,\ldots,n)$, we can get the next normalization condition for q_k as below:

$$\sum_{i=1}^{n} q_i = 1 \tag{7}$$

Equations (2-7) describe a compact model [3-4] with R_{thJ0}, a_i, q_k, $R_{i,k}$ parameters. Because of the model symmetry, and additional normalization conditions, eqn. (3) and (5), the total number of $(n+1)^2$ model parameters is reduced to fully independent ones, given by [3-4]

$$\frac{1}{2}(n-1)\cdot(n+4)+1 \tag{8}$$

where n is the number of boundary nodes of the heat source.

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As an example of applying compact modeling to power electronics, we present in this paper model of D2Pak enclosure (Fig. 1). Four boundary nodes were defined in the structure, i.e., metal pins (n_1), top of the ceramic case (n_{ob}), metal base (n_2) mounted on the PCB (Printed Circuit Board), and the bottom of PCB (n_{pd}). Silicon chip inside is the point where the power is generated.

A corresponding compact model in the form of a network is shown in Fig. 2.

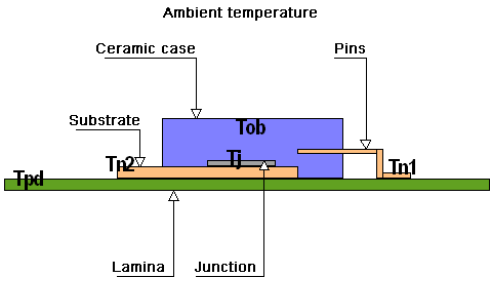

***Fig. 1**. D2Pak enclosure of power device with indicated nodes for compact model*

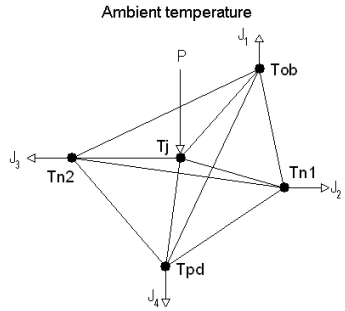

***Fig. 2**. Compact model of D2Pak,*
T_{ob} – case temperature,
T_{n1} – electrodes temperature ,
T_{n2} – metal radiator temperature,
T_{pd} – PCB temperature,
Tj – junction temperature

3. ANSYS simulations

Compact modeling in our work was supported by physical simulations. It is done mainly to determine the portion of power transferred through all nodes to the ambient. It is more explained in sections 4-5 in this paper.

The model is for MOSFET (Metal-Oxide-Semiconductor Field Effect Transistor) power transistor in D2Pak ceramic case. The model is built up using the manufacturer's data presented in Table 2.

***Table 2**.Material parameters of modeled device*

	Density [kg/m^3]	Specific heat [J/(kg·K)]	Thermal conductivity [W/(m·K)]
Cooper pins	8960	385	386
Silicon heat source	2330	710	150
Ceramic case	4000	300	20
PCB	2500	1000	5
Power generated in the source	0.75 – 1.5 W		
Ambient temperature	298.15 K		
Heat transfer coefficients	2 – 5 W/(m^2·K) (depending on the node)		

A mesh for finite element modeling using ANSYS5.7, and the exemplary results are presented in Fig. 3.

Temperature distribution in Fig. 3 is obtained for total power of 1.5 W generated in the structure, what is corresponding to uniform power density of 2.45*10^8 W/m^3 in silicon. Temperature of 416.9 K is on the top of the D2Pak case, while the maximum one in the junction is 421.6 K.

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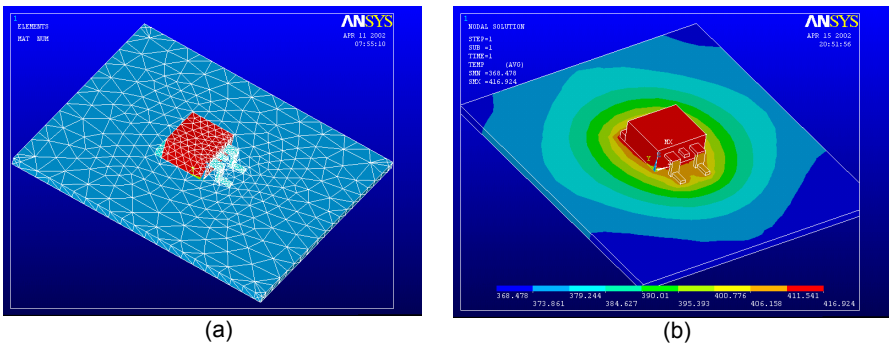

(a) (b)

Fig. 3. *Mesh for D2Pak enclosure (a), and temperature distribution (b), ANSYS5.7 modeling*

4. Compact model for D2Pak power device

The physical model in ANSYS is defined for getting average temperature on subsurfaces corresponding to considered points of the structure T_{n1}, T_{n2}, T_{pd}, T_{ob}. Additionally, simulation provides portions of power $J_1...J_4$ transferred to the ambient through the nodes. By solving linear equations (6) thermal resistances R_{thJ0}, $R_{i,k}$ as well as parameters a_i, q_k are obtained for a given total power P=0.75, 1, 1.25 and 1.5 W. Results are in table 3.

In order to validate the compact model, the results' comparison from both physical and compact modeling for different power P=0.6, 0.85, 1.1, 1.4, 1.75 W are performed. Temperature T_{n1}, T_{n2}, T_{pd}, T_{ob} *and* T_j are calculated for comparison as shown in Table 4, while their uncertainty are in Table 5.

Table 3. *Parameters of compact model obtained using data from physical simulation*

R_{thj0}	7,6356	$R_{Tn2\text{-}Tpd}$	1,06E+1
a_{Tn2}	1,667	$R_{Tn2\text{-}Tob}$	-5,43
a_{Tn1}	-1	$R_{Tn1\text{-}Tpd}$	-8,85
a_{Tpd}	5.55E-1	$R_{Tn1\text{-}Tob}$	9,94E+1
a_{Tob}	-2,22E-1	$R_{Tpd\text{-}Tob}$	9,53E+1
q_{Tn2}	6,77E-2		
q_{Tn1}	7,36E-1		
q_{Tpd}	-2,6E-2		
q_{Tob}	2,22E-1		
$R_{Tn1\text{-}Tn2}$	-1,719		

Table 4. *Junction temperature obtained by physical and compact modeling, ANS – ANSYS5.7, Compact – Compact thermal model*

P	[W]	0,6	0,85	1,1	1,4	1,75	
T_j-ANS	[K]	345,8	365,6	385,7	409,3	437,1	Fig. 5a
T_j-Compact		346,5	368,5	388,1	412,6	441,5	

Table 5. *Uncertainty of junction temperature T_j*

P [W]	0,6	0,85	1,1	1,4	1,75
σ [%]	1,5	4,3	2,7	3,0	3,2

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The measurement uncertainty is at the reasonable level for engineering practice, and the fast calculation is the main advantage of using compact modeling. It is possible to get junction temperature for different power generated in the device as well as for various boundary conditions, i.e.: different values of heat transfer coefficients.

5. Thermographic measurements

D2Pak device is a SMD (Surface Mounted Device) one. The metal pad below the component, where the element is soldered, contributes in cooling down the structure and can improve the heat transfer to the ambient. It acts as thermal spreader. The first modeling assume the different areas of the metal pad below the component. The maximum temperature of the junction is calculated. As shown below (Fig. 4), there is an improvement of device cooling, however after enlarging the pad's area above 50% of the component's area itself, the cooling down improvement is very small.

In order to verify the correctness of compact and physical modeling, thermographic measurements were performed. N-channel MOSFET power transistor were placed on the copper pad, which area was greater than the base of the component by 10%. Table 6 contains the results from ANSYS simulations and measurements.

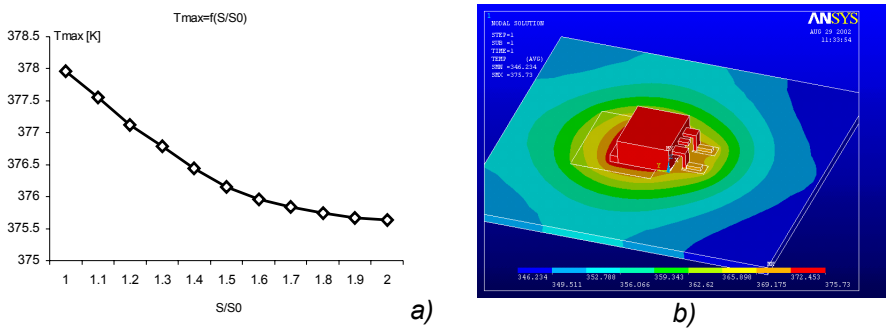

Fig. 4. *Maximum temperature versus S/S0, S – area of pad, S0 – area of metal base of the component*

Additionally, the results from simulation and measurement are presented in Fig. 5, and chosen thermal images are in Fig. 6. For higher power, the characteristics obtained by measurements and simulation differ from each other. Heat transfer coefficients for upper and lower parts of the structure were chosen according the literature recommendations. The cooling conditions in the experiments were different in simulations and measurements. It is possible to match both results by choosing the proper heat transfer coefficients. Such an approach needs to use the optimization procedure.

Table 6. *Maximum and minimum temperature – ANSYS simulations and measurements*

Results from ANSYS				
P [W]	0,75	1	1,5	2
T_{max} [K]	358,4	377,9	416,9	455,9
T_{min} [K]	358,2	377,5	416,3	455,1
Results from thermal camera measurements				
P [W]	0,7803	1,08	1,5123	1,92
T_{max} [K]	356,5	373,4	396,1	423,1
T_{min} [K]	332,4	349,7	370,1	385,1

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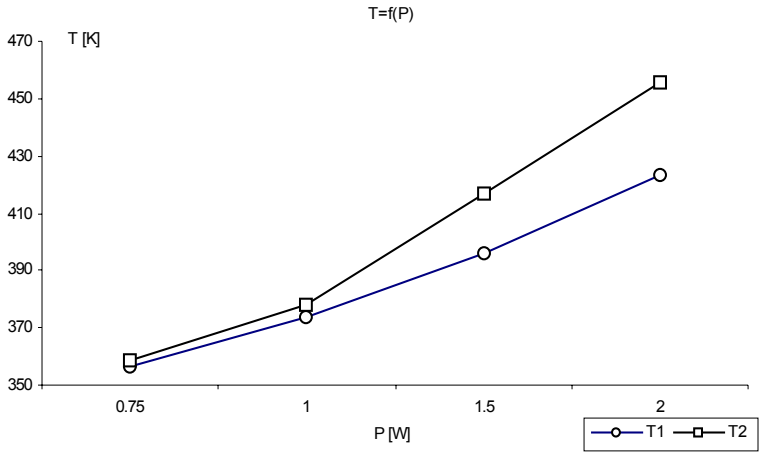

Fig. 5. *Maximum temperature obtained by ANSYS simulations (T2) and thermographic measurements (T1)*

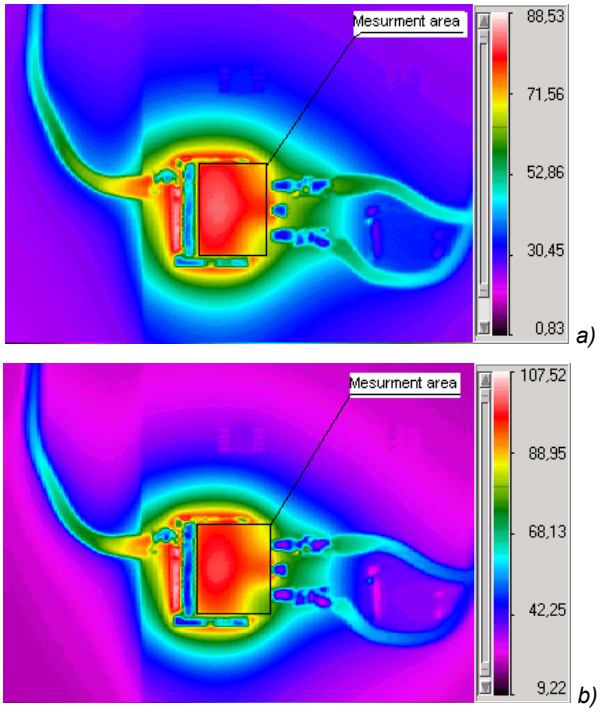

Fig. 6. *Temperature distributions, a) P=0.78 W, T_{max}=356.5 K, b) P=1.08 W, T_{max}=373.5 K*

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6. Conclusions

Compact model of power electronic device in D2Pak is presented in this work. It has been shown that from physical modeling using advanced simulation software it is possible to find the portions of total power dissipated to the ambient through all nodes. These parameters are responsible for boundary conditions and are necessary for calculations model parameters. Thermography measurements have been used for verifying the model correctness.

Additionally, the influence of the area of metal pad on PCB under the power device in power dissipation to the ambient and cooling down the whole structure has been taken into account. It was proved by simulation, that the area above 50% of the device area do not improve cooling significantly.

Compact modeling is the powerful engineering tool for fast and acceptable calculations. Accuracy of such modeling can be improved by increasing number of boundary nodes, and thermography measurements. The problem of boundary conditions are solved either by physical simulation or by thermal measurements.

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